REMARKS

The allowance of claims 6 – 23 is noted with appreciation. Dependent claims 2 – 5, 26 and 27, indicated to be allowable, are being rewritten in independent form so that there is no question that they are now also now allowable. Withdrawn claims 28 – 33 are being cancelled.

The rejection of claim 1 as anticipated under 35 U.S.C. § 102(b) by U.S. patent no. 5,278,438 (Kim et al.) is respectfully traversed. Claim 1 recites "isolation trenches formed in the substrate between and *surrounding* the individual stacks," (emphasis added). The Office Action points to isolation trenches 30 and 42 of the Kim et al. patent as "surrounding" the cells 20, which are taken to be the claimed individual stacks. Although, as best seen from Figure 13, the trenches 30 and 42 are on opposite sides of the cells 20. They do not surround the cells 20. It is respectfully submitted that one ordinarily skilled in the art would consider the term "surround" to mean that trenches extend all the way around the cells 20; that they are on all sides of the cells 20. This is consistent with common dictionary definitions of the term "surround." This is not found in the Kim et al. patent.

The rejection of claims 24 and 25 under 35 U.S.C. § 102(b) by U.S. patent no. 5,071,782 (Mori) is also respectfull y traversed. These claims recite "a rectangular array of charge storage elements formed across a surface of the substrate" that the Mori patent does not describe. Rather, in the Mori patent, the floating gates FG are formed in trenches 22 within the substrate, not across its surface. The Office Action contends that elements 20 are the claimed "charge storage elements" but rather the reference number "20" is used to identify an entire memory cell (see, for example, Mori patent col. 4, lns. 45-46 and col. 5, ln. 48). This distinction alone is submitted to render claims 24 and 25 patentable.

But in addition, it is not seen that the Mori patent suggests "select transistor gates" as recited in the last paragraph of claim 24. A select transistor is formed by a channel region within a semiconductor substrate across which a conductive select transistor gate extends, with a layer of gate dielectric between them. A select transistor is formed in series with a charge storage memory cell, between source and drain substrate regions, and operates to connect or disconnect the memory cell from access circuits. It does this by a control of the voltage on the select gate. Examples of select gates are shown in Figures 10, 12, 14 and 15 of the present application. The regions of the substrate within the trenches, opposite a dielectric layer between them, form the channels whose conduction is controlled by the voltage on the select gate.

No select transistor gates can be found in the Mori patent. The Office Action identifies the floating gates FG as the claimed "select transistor gates," but this is respectfully submitted to be incorrect. The floating gates FG are indeed floating in voltage. Nothing is connected to them to drive them to a certain voltage to operate as a select transistor. They cannot operate to selectively connect a memory cell to access circuits of the memory. The "select transistor gates" limitation of claims 24 and 25 therefore also gives them novelty.

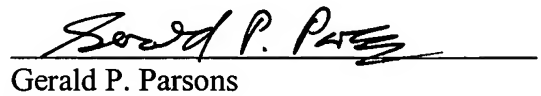
Information Disclosure Statement

A Supplemental Information Disclosure Statement is being filed herewith to provide the Examiner the International Search Report and The Written Opinion of the European Patent Office, with references cited, for the PCT application corresponding to the present U.S. application. Consideration of these documents and making them of record in the file of the present application are respectfully requested.

Conclusion

Accordingly, it is believed that this application is now in condition for allowance and an early indication of its allowance is solicited. However, if the Examiner has any further matters that need to be resolved, a telephone call to the undersigned attorney at 415-318-1163 would be appreciated.

Respectfully submitted,



July 13, 2005

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